

LISTING OF THE CLAIMS

Please amend the claims as shown below. Claims 1, 7, 13 and 19 are amended herein. This listing of the claims replaces all previous listings thereof.

1. (Currently Amended) A clock signal duty cycle stabilization circuit, comprising:
- an edge detection circuit having a first delay and configured to receive an external clock signal and generate an output therefrom; and
- a ~~latch circuit~~ non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator coupled to receive a first signal comprising the output from the edge detection circuit and a second signal comprising an output from a conditioning circuit, the ~~latch circuit~~ non-overlapping clock generator configured to produce an internal clock signal having a rising edge generated with the first signal and a falling edge generated with the second signal wherein the internal clock signal has a duty cycle that is independent of the duty cycle of the external clock, the non-overlapping clock generator further configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal;
- wherein the first delay is equal to or greater than the second delay.

2. (Original) The clock signal duty cycle stabilization circuit of claim 1, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate

having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

3. (Currently Amended) The clock signal duty cycle stabilization circuit of claim 1, wherein the ~~latch circuit~~ non-overlapping clock generator comprises ~~an R-S~~ a delayed latch, the ~~R-S~~ delayed latch configured to receive the output of the edge detection circuit and generate the rising edge and the falling edge therefrom.

4. (Cancelled)

5. (Original) The clock signal duty cycle stabilization circuit of claim 1, wherein the external clock signal is a reference clock signal from an external source.

6. (Original) The clock signal duty cycle stabilization circuit of claim 1, wherein the internal clock signal is a 50% duty cycle clock signal for use by an analog to digital converter.

7. (Currently Amended) An analog to digital converter system, comprising:
an switched-capacitor analog to digital converter circuit for converting analog signals into digital signals;
a clock signal duty cycle stabilization circuit coupled to the analog to digital converter circuit, the clock signal duty cycle stabilization circuit configured to produce an

internal clock signal for use by the analog to digital converter circuit wherein the internal clock signal has a duty cycle that is independent of the duty cycle of the external clock, the clock signal duty cycle stabilization circuit further comprising:

an edge detection circuit having a first delay and configured to receive the external clock signal and generate an output therefrom; ~~and~~

a conditioning circuit for producing a conditioned signal having a one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

~~a latch circuit~~ non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator coupled to receive a first signal comprising the output from the edge detection circuit and to receive a second signal comprising the conditioned signal, ~~the latch circuit~~ non-overlapping clock generator configured to produce a rising edge of the internal clock signal and a falling edge of the internal clock signal in accordance with the second signal, the non-overlapping clock generator further configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal;

wherein the first delay is equal to or greater than the second delay.

8. (Original) The system of claim 7, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

9. (Currently Amended) The system of claim 7, wherein the ~~latch circuit~~ non-overlapping clock generator comprises ~~an R-S~~ a delayed latch, the ~~R-S~~ delayed latch configured to receive the output of the edge detection circuit and generate the rising edge and the falling edge therefrom.

10. (Cancelled)

11. (Original) The system of claim 7, wherein the external clock signal is a reference clock signal from an external source.

12. (Original) The system of claim 7, wherein the internal clock signal is a 50% internal clock signal for use by an analog to digital converter.

13. (Currently Amended) A clock signal duty cycle stabilization circuit, comprising:

an edge detection circuit having a first delay and configured to receive an external clock signal and generate an output therefrom;

a VCRO circuit for producing a VCRO signal having one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

a ~~timing generator circuit~~ non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator coupled to receive the output from the edge detection circuit, the ~~timing generator circuit~~ non-overlapping clock

generator configured to produce an internal clock signal in accordance with a setting and resetting of the ~~timing-generator circuit~~ non-overlapping clock generator in accordance with a first signal and a second signal, the first signal comprising the output of the edge detection circuit and the second signal comprising the VCRO signal, wherein the rising edge of the external clock sets ~~the timing-generator~~ non-overlapping clock generator to produce a rising edge of the internal clock signal and the VCRO signal resets the ~~timing-generator circuit~~ non-overlapping clock generator to produce a falling edge of the internal clock signal wherein the internal clock signal has a duty cycle that is independent of the duty cycle of the external clock, the non-overlapping clock generator further configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal;

wherein the first delay is equal to or greater than the second delay.

14. (Original) The clock signal duty cycle stabilization circuit of claim 13, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

15. (Original) The clock signal duty cycle stabilization circuit of claim 13, wherein the ~~timing-generator circuit comprises a non overlapping clock generator~~ comprises a delayed latch, the ~~non-overlapping clock generator~~ delayed latch configured to receive the output of the edge detection circuit and generate a rising edge of the internal clock signal therefrom.

16. (Cancelled)

17. (Original) The clock signal duty cycle stabilization circuit of claim 13, wherein the external clock signal is a reference clock signal from an external source.

18. (Original) The clock signal duty cycle stabilization circuit of claim 13, wherein the internal clock signal is for use by an analog to digital converter coupled to the clock signal duty cycle stabilization circuit.

19. (Currently Amended) An analog to digital converter system, comprising:
an analog to digital converter circuit for converting analog signals into digital signals;
a clock signal duty cycle stabilization circuit coupled to the analog to digital converter circuit, the clock signal duty cycle stabilization circuit configured to produce an internal clock signal for use by the analog to digital converter circuit, the clock signal duty cycle stabilization circuit further comprising:

an edge detection circuit having a first delay and configured to receive an external clock signal and generate an output therefrom; and

a VCRO circuit for producing a VCRO signal having one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

~~a timing generator circuit~~ non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator coupled to receive the

output from the edge detection circuit, the ~~timing generator circuit~~ non-overlapping clock generator configured to produce an internal clock signal in accordance with a setting and resetting of the timing generator circuit in accordance with a first signal and a second signal, the first signal comprising the output of the edge detection circuit and the second signal comprising the VCRO signal, wherein the rising edge of the external clock sets the ~~timing generator~~ non-overlapping clock generator to produce a rising edge of the internal clock signal and the VCRO signal resets the ~~timing generator circuit~~ non-overlapping clock generator to produce a falling edge of the internal clock signal wherein said internal clock signal has a duty cycle that is independent of the duty cycle of said external clock, the non-overlapping clock generator further configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal;

wherein the first delay is equal to or greater than the second delay.

20. (Original) The system of claim 19, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

21. (Original) The system of claim 19, wherein the ~~timing generator circuit~~ comprises a non overlapping clock generator comprises a delayed latch, the ~~non-overlapping clock generator~~ delayed latch configured to receive the output of the edge detection circuit and generate a rising edge of the internal clock signal therefrom.

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22. (Cancelled)

23. (Original) The system of claim 19, wherein the external clock signal is a reference clock signal from an external source.

24. (Cancelled)